Complementary N- and P-Channel MOSFET Half-Bridge

CHARACTERISTICS

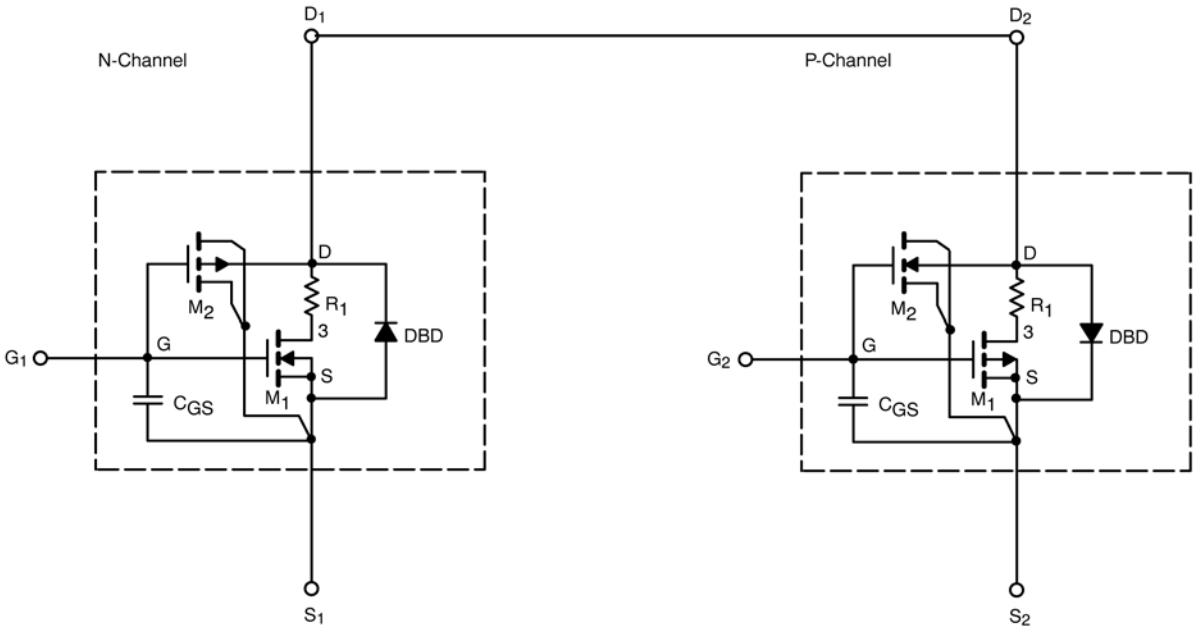
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



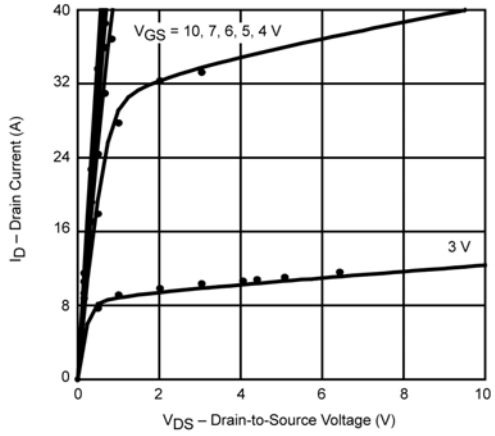
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

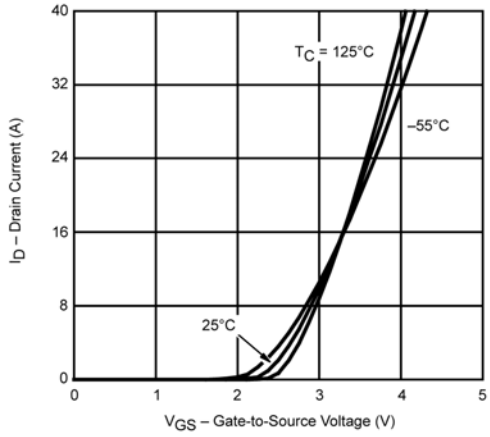
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	1.4		A
		V_{DS} = V_{GS}, I_D = –250 μA	P-Ch	0.87		
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	N-Ch	273		
		V_{DS} = –5 V, V_{GS} = – 4.5 V	P-Ch	64		
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 8.8 A	N-Ch	0.014	0.015	Ω
		V_{GS} = –4.5 V, I_D = –5.7 A	P-Ch	0.032	0.030	
		V_{GS} = 4.5 V, I_D = 7 A	N-Ch	0.020	0.022	
		V_{GS} = –2.5 V, I_D = –4.8 A	P-Ch	0.052	0.048	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 8.8 A	N-Ch	21	18	S
		V_{DS} = –15 V, I_D = –5.7 A	P-Ch	16	12	
Diode Forward Voltage[a]	V_{SD}	I_S = 1.8 A, V_{GS} = 0 V	N-Ch	0.72	0.73	V
		I_S = –1.8 A, V_{GS} = 0 V	P-Ch	0.81	– 0.75	
Dynamic[b]						
Total Gate Charge	Q_g	N-Channel V_{DS} = 15 V, V_{GS} = 5 V, I_D = 8.8 A P-Channel V_{DS} = –4 V, V_{GS} = –5 V, I_D = –5.7 A	N-Ch	11.8	11.5	nC
			P-Ch	13.3	13.5	
Gate-Source Charge	Q_{gs}		N-Ch	3	3	
			P-Ch	2.2	2.2	
Gate-Source Charge	Q_{gs}		N-Ch	4	4	
			P-Ch	3	3	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} =15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = –4 V, R_L = 4 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω	N-Ch	12	15	ns
			P-Ch	26	21	
Rise Time	t_r		N-Ch	10	8	
			P-Ch	31	45	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch	17	35	
			P-Ch	23	60	
Fall Time	t_f		N-Ch	17	10	
			P-Ch	39	55	
Source-Drain Reverse Recovery Time	t_{rr}	I_S = 1.8 A, di/dt = 100 A/μs	N-Ch	22	30	
			P-Ch	34	50	

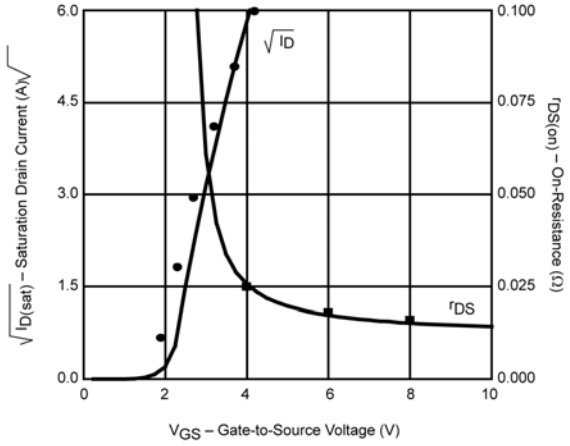
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

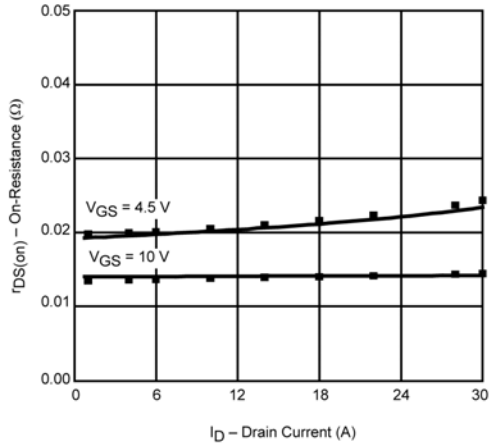
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

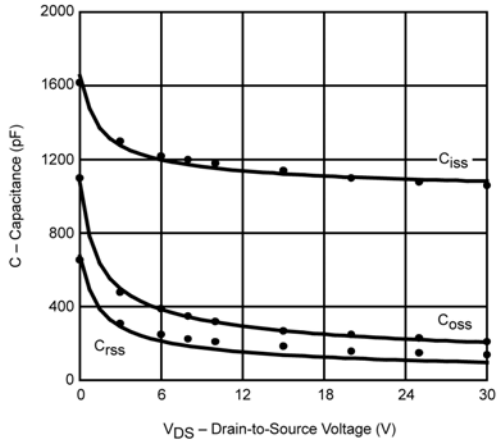
N-Channel MOSFET

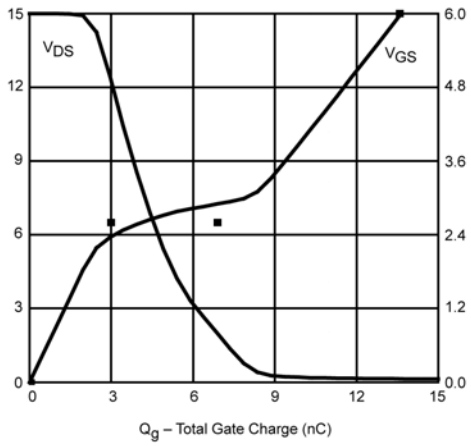






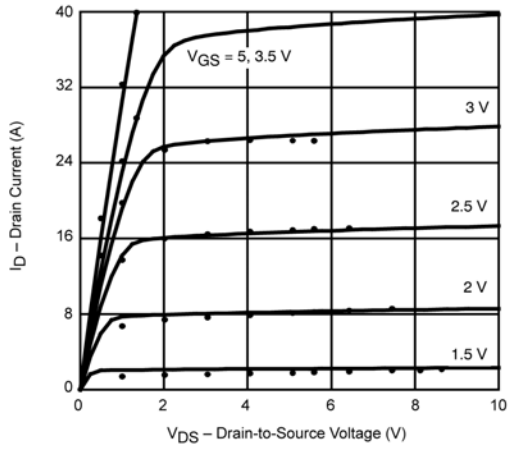


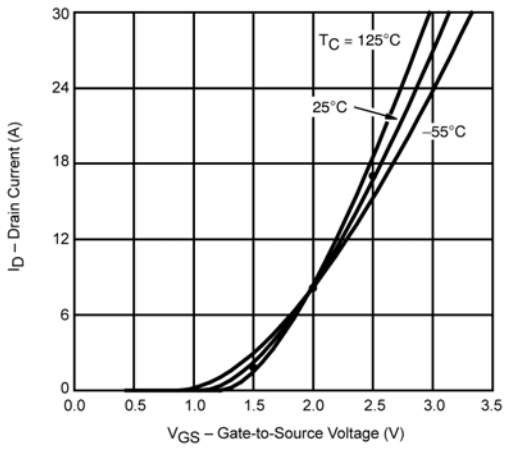


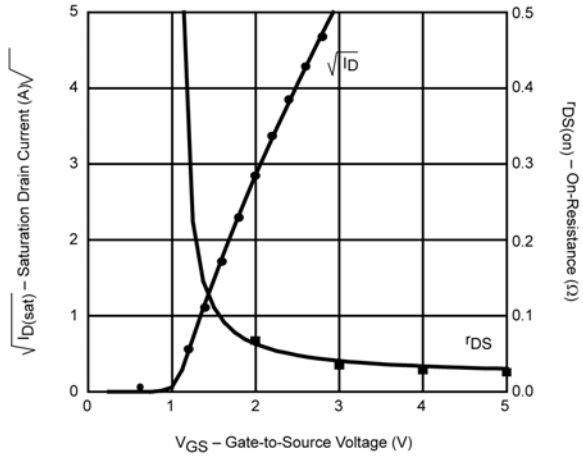


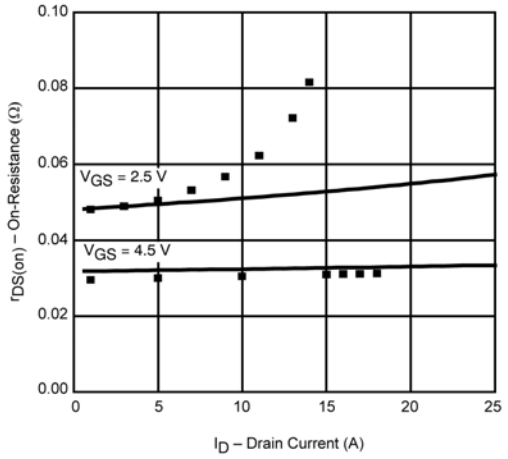
Note: Dots and squares represent measured data.

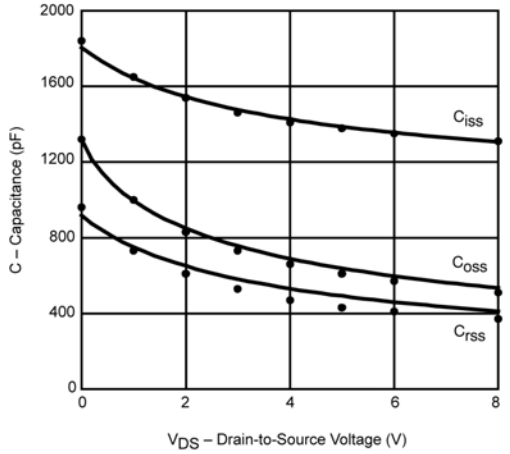
P-Channel MOSFET

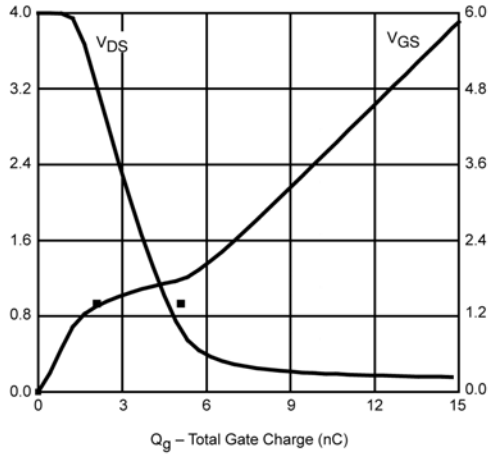












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